Nikita Lazarev | CV

Aurora Street – Ithaca – NY, USA
+16073790757 • nl524@cornell.edu

Research Interests

Computer Hardware: Networking Hardware, SmartNICs, FPGAs, System Interconnects
Computer Systems: Networking and Distributed Systems, Kernel Bypass Technologies
Application Domains: Low-Latency Systems, Datacenter Systems, 5G and vRAN

Current Research Focus: (1) Pushing further and making practical the tight integration of datacenter machines via closely-coupled with processors FPGAs; (2) Making 5G vRAN stacks as a cloud native feature by leveraging advances in low-latency networking and realtime distributed systems.

Education

Cornell University **Ithaca, NY, USA**
Computer Engineering: PhD *2019–*

Swiss Federal Institute of Technology (EPFL) **Lausanne, Switzerland**
Computer Science: MS *2016–2018*

Bauman Moscow State Technical University **Moscow, Russia**
Electrical Engineering & Robotics: Engineer *2010–2016*

Research Experience

Industry

Microsoft Azure for Operators Research (part-time researcher) **Redmond, WA, USA**
Layer disaggregation and workload migration in 5G/vRAN stacks *06.2021 - now*

Research and development towards enabling MAC/PHY layer disaggregation and 5G workload migration in the future Azure vRAN infrastructure. I developed a DPDK-based component for the layer disaggregation, and implemented and tested cell migration logic in FlexRAN, both in local and distributed settings under the real 5G workload.

Microsoft Research, Systems and Networking lab (internship) **Cambridge, UK**
FPGA-based implementation of a transport network layer for the specific workload *06.2018 - 09.2018*

Fork of the Microsoft FaRM project. The goal is to design a CPU-free datastore architecture for the applications in distributed graph databases and key-value stores. Such applications cause intense network traffic composed of small randomly addressed packets, and my task was to design the transport layer adopted for such workload. As the result, the network performance was improved by 30% in comparison with the previously used transport layer.

Microsoft Research, Systems lab (internship) **Bangalore, India**
Hardware acceleration of real-time IoT AI algorithms *08.2017 - 02.2018*

Two ML algorithms have been optimized at MSRI in order to fit on resource-constrained IoT devices. In this project, I was working on a design of an FPGA-based heterogeneous SoC for efficient implementation of those optimized algorithms in hardware. The designed SoC enables low-latency implementation of the algorithms, and it is generic: both algorithms can be implemented leveraging exposed SW interfaces without changing the hardware.

Samsung Research Center (part-time) **Moscow, Russia**
Junior software developer: compiler technologies and systems *2014 - 2016*

Android ART compiler and runtime optimization. Focus on compiler optimization: loop transformations, division optimization, heterogeneous back-end support. Focus on runtime optimization: hash tables for Java strings. Research focus: speed-up of class loading by static analysis of the class references.

Academia

Cornell University **Ithaca, NY, USA**
Independent research, supervisor: Prof. Zhiru Zhang, Prof. Christina Delimitrou *02.2020 -*
FPGAs in datacenters: exploring the opportunities of closely-coupled FPGAs for improving networking performance and acceleration of datacenter tax functions.

Swiss Federal Institute of Technology (EPFL) **Lausanne, Switzerland**
Term project, supervisor: Prof. Babak Falsafi *02.2018 - 07.2018*
Development of a lightweight VLIW-like SIMD core for a neural processor

Swiss Federal Institute of Technology (EPFL) **Lausanne, Switzerland**
Research assistantship: setup of a quantum mechanics experiment *02.2017 - 07.2017*
Development and production of a fast FPGA-based PID control system for lasers

Bauman Moscow State Technical University **Moscow, Russia**
Term project *2013 - 2014*
Phasechronometric measurement device: FPGA programming and PCB design

Lomonosov Moscow State University **Moscow, Russia**
Independent project *2012 - 2013*
Brain - computer interface: RF-PCB design, microcontroller firmware development, deep learning

Teaching Experience

Cornell University **Ithaca, NY, USA**
Digital logic and computer organization (ECE-2300): teaching assistant *2021*
Keywords: computer architecture, FPGA, Verilog

EPFL **Lausanne, Switzerland**
Real-time embedded systems (CS-476): teaching assistant *2018*
Keywords: FPGA, hardware accelerator, VHDL

Microsoft Research **Bangalore, India**
Tutorial: introduction to FPGAs *2017*
Keywords: FPGA, hardware accelerator

Bauman Moscow State Technical University **Moscow, Russia**
Implementation of control systems: guest lecturer *2015*
Keywords: control systems, PID, microcontrollers

Key implementation skills

Software skills

Top programming languages: C++, Python, C, Scala, Java

Domains: Kernel bypass networking, distributed systems, vRAN and 5G, realtime and embedded systems, machine learning, compiler optimization and runtime systems

Hardware skills

RTL languages: System Verilog, VHDL, Chisel

HLS languages: SystemC

Domains: SmartNICs and networking devices, AI accelerators

Key research/theoretical skills

Theory of algorithms, distributed systems, computer systems, machine learning, probability and statistics, complexity theory, basics of signal processing and control, basics of game theory

Languages

Russian: Mother tongue

English: Fluent

French: Elementary

Selected Publications

- **A Roadmap for Enabling a Future-Proof In-Network Computing Data Plane Ecosystem**
  D. Kim, N. Lazarev, T. Tracy, F. Siddique, H. Namkung, J. Hoe, V. Sekar, K. Skadron, Z. Zhang, S. Seshan
  Arxiv pre-print, October, 2021
- **Dagger: Efficient and Fast RPCs in Cloud Mcroservices with Near-Memory Reconfigurable NICs**
  Nikita Lazarev, Neil Adit, Shaojie Xiang, Zhiru Zhang, Christina Delimitrou
  ASPLOS'21, April, 2021
- **Dagger: Towards Efficient RPCs in Cloud Microservices with Near-Memory Reconfigurable NICs**
  Nikita Lazarev, Neil Adit, Shaojie Xiang, Zhiru Zhang, Christina Delimitrou
  IEEE Computer Architecture Letters, August, 2020
- **Phase-Chronometric System for Monitoring Turning Processes**
  D. Boldasov, N. Lazarev, A. Syritsky
  The Devices (in Russian), May, 2015

Patents

- **Precise FPGA-based time measurement system for real-time turning process monitoring**
  A. Syritsky, D. Boldasov, N. Lazarev, A. Komshin
  Registration number: RU2019610688

Achievements

- IEEE Micro "Top Picks from the Computer Architecture Conferences": Honorable Mention, 2022
- Cornell University Graduate Research Fellowship (Jacobs Scholarship), 2019
- Russian Presidential Scholarship, 2016
- Medal for Excellent Graduation, 2016
- Samsung R&D "Above and Beyond" Award, 2015
- 2nd Place on the National Olympiad for Physics and Mathematics, 2010
- 1st Place on the Regional Competition of Programming Projects for High School Students, 2010